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EXAMINER	
CHANG, EDITH M	
ART UNIT	**PAPER NUMBER**
2634	

DATE MAILED: 04/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/382,459	DEDIC ET AL.	
	Examiner	Art Unit	
	Edith M Chang	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *33* is/are allowed.

6)☒ Claim(s) *27-32 and 39* is/are rejected.

7)☒ Claim(s) *1-26,34-38 and 40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 August 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed February 2 2004 have been fully considered but they are not persuasive.

Argument:

Claim 30, Rising Edge of Third Clock Signal At Substantially Same Time As Rising Edge Of First Clock Signal Not Described. Hata describes that the rising edge of a third clock signal is not at substantially a same time, but rather is substantially delayed relative to the rising edge of a first clock signal.

Response:

Hata's third clock signal is slightly delaying with respect to edges of the clock CLKin (column 15 lines 1-2) wherein slightly delaying/advancing is substantially a same time. The control circuit of Hata's circuit has CLKin as the input, the output is controlled by the rising edge of the CLKin (FIG.8, CLKin is applied at a, the output of 20/21 is controlled by the edge of CLKin as shown in FIG.6 DIGCLK to 40 of the instant application). Hata discloses the limitations recited in the claim.

Argument:

Claim 30, Input Signal Processing Circuit Performing A Predetermined Processing Operation On a First Signal Not Described. Claim 30 recites a feature of a first latch circuit inputting an output signal of an input signal processing circuit.

Response:

Claim 30 recites a digital circuit, comprising: an input signal processing circuit, inputting one or more first signal(s), and performing a predetermined processing operation on the first signal(s). Hata discloses a digital circuit (2 FIG.1/FIG.12) comprising an input signal processing circuit (FIG.14), inputting one or more first signal(s) (Din FIG.14), and performing a predetermined processing operation on the first signal(s) (the input signal processing circuit predetermined the processing operation on the first signal).

Argument:

Claim 39, Data Signals Not Described. A plurality of digital signals received by the digital input circuit described in Bechade are simply delayed versions of a first clock signal. Digital data signals are not described in Bechade

Response:

The signal 13 of fig.1 received by the digital input circuit described in Bechade is the digital data signals input to the data input circuit/pulse generators (14 fig.1). Delayed versions of a first clock signal are generated as the digital data signals to the pulse generators.

The rejections of claims 30-32 and 39 are upheld, and new ground rejections of claims 27-29 are as follow:

Claim Objections

2. Claims 1-22, 23-26, 34-35, 36-38, and 40 are objected to because of the following informalities:

Claim 1, line 1, "Digital circuitry" should be "A digital circuitry"; line 19, "clock generating circuitry" should be "a clock generating circuitry".

Claims 2-22, line 1, "Digital circuitry" should be "The digital circuitry".

Claim 5, line 2, "a predetermined enabling change enabling" is suggested changing to "a predetermined enabling change enabling in said first clock signal".

Claim 7, line 5, "with a delayed version" should be "with the delayed version"; line 6, "said enabling change in the third clock signal" should be "said predetermined enabling change in the third clock signal; line 7, "said enabling change in the first clock signal" should be "said predetermined enabling change in the first clock signal"; line 7, "said disabling change" should be "said predetermined disabling change".

Claim 8, line 3, "a include delay balancing element" should be "a delay balancing element".

Claim 9, line 9, "signal processing circuitry" should be "a signal processing circuitry"; line 10, "one or more changed and unchanged basic clock signal (s)." should be "one or more changed basic clock signal(s) and said one or more basic clock signal(s)."

Claim 12, line 2, "second signal(s), said one or more first" should be "second signal(s), or said one or more first"; line 3, "output signal(s), and said one or more second signal(s)" should be "output signal(s), or said one or more second signal(s)"; line 4, "is/are" should be "is" to clearly indicated the least one signal pair.

Claim 13, line 2, "or each at least " should be "at least", "first signal(s), and said one or more second" should be "first signal(s), or said one or more second", line 4 "signal(s), and said one or more output signal(s)" should be "signal(s), or said one or more output signal(s)" to clearly indicate the least one.

Claim 16, line 3, "said circuit units" is suggest changing to "said individual circuit units"; line 6, "said circuit unit(s)" is suggest changing to "said individual circuit unit(s)", "said local clock driver" should be "said local clock drivers"; line 9, "corresponding circuit unit(s)" is suggest changing to "corresponding individual circuit unit(s)"

Claim 17, line 1, "each said circuit unit" is suggest changing to "each said individual circuit units".

Claim 18, line 4, "signals" should be "signal", "said plurality" should be "said plurality of local clock drivers" or "said plurality of individual circuit units" to clarify the invention.

Claim 19, line 2, "the plurality of circuit units" should be "the plurality of individual circuit units", "said power supply" should be "power supplies"

Claim 20, line 4, "said circuit unit" lacks antecedence.

Claim 21, line 2, "said circuit unit" lacks antecedence.

Claim 22, line 2, "plurality of circuit units" should be "the plurality of individual circuit units", "each said power supply" is suggest changing to "each power supply"; line 7, "said circuit unit" should be "said circuit unit(s)"

Claim 23, line 1, "Mixed-signal circuitry" should be "A mixed-signal circuitry";

line 2, "digital circuitry" should be "a digital circuitry"; line 20, "clock generating circuitry" should be "a clock generating circuitry"; line 27, "analog circuitry" should be " an analog circuitry".

Claims 24-26, line 1, "Mixed-signal circuitry" should be "The mixed-signal circuitry".

Claim 25, line 5, "said one or more output signal(s)" should be "said received one or more output signal(s)".

Claim 26, line 3, "power supply circuitry" should be "a power supply circuitry"; line 4, "to at least a second part" should be "to a second part"; line 7, "said second clocked means" lacks antecedence.

Claim 34, line 4, "a delayed version" should be "the delayed version".

Claim 36, line 13, "shorter delay time then the delay time of" should be "shorter delay time than the delay time of"

Claim 37, line 5, "a delayed version" should be "the delayed version".

Appropriate corrections are required.

Claim 40, lines 10 and 12, "the output signal" should be "an output signal".

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 27-29, and 30-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Hata (US Patent 5479455).

Regarding **claim 27**, Hata discloses a digital circuit (FIG.1) comprising: an input signal processing circuit (2 FIG.1) clocked by a first clock signal (CLK FIG.1), inputting one or more first signal(s) (Din FIG.1), and performing a predetermined processing operation on the first signal(s); a first latch circuit (9b FIG.14) clocked by a second clock signal (CLKb FIG.14), and inputting an output signal from the input signal processing circuit (Din FIG.14); a second latch circuit (9a FIG.14) clocked by a third clock signal (CLKa FIG.14), and inputting an output signal (a FIG.14) from the first latch circuit; and a clock generating circuit (6 FIG.4) generating the second and third clock signals from the first clock signal (CLKin FIG.14), the second clock signal being delayed relative to the first clock signal by a predetermined delay time (CLKb FIG.15, where the second rising edge of CLKb is delayed from the first rising edge of CLKin), and a rising edge of the third clock signal occurring at substantially a same time as a rising edge of the first clock signal (CLKa FIG.15, wherein the first rising edge of CLKa occurs substantially a same time of the first rising edge of CLKin), and a falling edge of the third clock signal (any falling edge such as the second falling edge of the CLKa is the "a falling edge") occurring at substantially the same time as a rising edge of the second clock signal (a corresponding rising edge such as the second falling edge of the CLKb is the "a rising edge).

Regarding **claim 30**, Hata discloses a digital circuit (FIG.1) comprising: an input signal processing circuit (2 FIG.1) clocked by a first clock signal (CLK FIG.1), inputting one or more first signal(s) (Din FIG.1), and performing a predetermined processing operation on the first signal(s); a first latch circuit (9b FIG.14) clocked by a second clock signal (CLKb FIG.14), and

inputting an output signal from the input signal processing circuit (Din FIG.14); a second latch circuit (9a FIG.14) clocked by a third clock signal (CLKa FIG.14), and inputting an output signal (a FIG.14) from the first latch circuit; and a clock generating circuit (6 FIG.4) generating the second and third clock signals from the first clock signal (CLKin FIG.14), the second clock signal being delayed relative to the first clock signal by a predetermined delay time (CLKb FIG.15, where the second rising edge of CLKb is delayed from the first rising edge of CLKin), and a rising edge of the third clock signal occurring at substantially a same time as a rising edge of the first clock signal (CLKa FIG.15, wherein the first rising edge of CLKa occurs substantially a same time of the first rising edge of CLKin) and enabling the second latch circuit to enter a responsive state during a non-responsive state of the first latch circuit (CLKa & CLKb FIG.15, wherein the CLKa is high/enabled while the CLKb is low).

Regarding **claims 28 & 31**, Hata discloses the clock generating circuit comprises: a delay element (18 FIG.19) delaying the first clock signal (a FIG.19) to produce a delayed version thereof (c FIG.19), and a logic element (28 FIG.19) logically combining the first clock signal with the/a delayed version thereof such that an enabling change in the third clock signal (e FIG.19) occurs substantially simultaneously with an enabling change in the first clock signal (e & a FIG.21, where the first rising edge of e occurs substantially simultaneously with the first rising edge of a), and a disabling change in the third clock signal occurs substantially simultaneously with a change in the delayed version of the first clock signal (c & a FIG.21, where the second falling edge of e occurs substantially simultaneously with the fourth falling edge in c).

Regarding **claims 29 & 32**, Hata discloses clock generating circuit (6 FIG.14, FIG.19) further comprises: a delay balancing element (28-30 FIG.19) connected between said delay element (18 FIG.19) and said first latch circuit (6-9b FIG.14) receiving said delayed version of the first clock signal (c FIG.19) and deriving therefrom said second clock signal (CLKb FIG.14), and the delay balancing element having a first propagation delay between said change in the delayed version of the first clock signal and a predetermined enabling change in said second clock signal enabling/causing the first latch circuit to change from a non-responsive state to a responsive state (in FIG.21 the delay from the first falling edge of a and the first falling edge of c/delayed version is about one and one third interval, in FIG.15 the delay of enabling the CLKb/first latch is about one and one fourth interval wherein the first rising edge of CLKin to the second rising edge of CLKb, so there is a propagation delay) , said logic element having a second propagation delay between said change in said delayed version of the first clock signal and said disabling change in the third clock signal, and said first propagation delay being substantially equal to said second propagation delay (The logical element is 28 FIG.19, the balancing element is 28-30 FIG.19, the propagation delays is substantially equal as the clock generating circuit/control signal circuit construct in 6-9b, 6-9a FIG.14 and FIG.19 the detail construction of 6 FIG.14).

5. Claim 39 is rejected under 35 U.S.C. 102(b) as being anticipated by Bechade et al. (US Patent 5272729).

Regarding **claim 39**, Bechade et al. discloses a digital circuit (fig.1), comprising: a digital input circuit (14 fig.1) receiving a plurality of digital signals (13 fig.1) in response to a first clock

signal (EXTERNAL CLOCK fig.1); a delay element (12 fig.1) receiving the first clock signal and outputting a delayed clock signal (13 fig.1); a clock generating circuit (13-14-18-23 fig.1) receiving the first clock signal and generating a second clock signal (output of 18/input of 16 fig.1), produced from the delayed clock signal (13 fig.1), and a third clock signal (23 fig.1), produced from the first clock signal and the delayed clock signal (11'' fig.1); a first latch circuit (16 fig.1), coupled to the digital input circuit, receiving the output signal from the digital input circuit in response to the second clock signal (18 fig.1); and a second latch circuit (19 fig.1), coupled to the first latch circuit, receiving the output signal from the first latch circuit in response to the third clock signal (23 fig.1).

Allowable Subject Matter

6. Claim 33 is allowed.

7. Claims 1-26, 34-35, and 36-38, 40 are objected to informality, but would be allowable if rewritten to overcome the objections.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edith M Chang whose telephone number is 703-305-3416. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Edith Chang
April 15, 2004

CHIEH M. FAN
PRIMARY EXAMINER